

High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting (Prentice Hall Modern Semiconductor Design Series)

Kyung Suk (Dan) Oh, Xing Chao (Chuck) Yuan



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High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting (Prentice Hall Modern Semiconductor Design Series) Kyung Suk (Dan) Oh, Xing Chao (Chuck) Yuan New System-Level Techniques for Optimizing Signal/Power Integrity in High-Speed Interfaces--from Pioneering Innovators at Rambus, Stanford, Berkeley, and MIT

As data communication rates accelerate well into the multi-gigahertz range, ensuring signal integrity both on- and off-chip has become crucial. Signal integrity can no longer be addressed solely through improvements in package or board-level design: Diverse engineering teams must work together closely from the earliest design stages to identify the best system-level solutions. In High-Speed Signaling, several of the field's most respected practitioners and researchers introduce cutting-edge modeling, simulation, and optimization techniques for meeting this challenge.

Edited by pioneering experts Drs. Dan Oh and Chuck Yuan, these contributors explain why noise and jitter are no longer separable, demonstrate how to model their increasingly complex interactions, and thoroughly introduce a new simulation methodology for predicting link-level performance with unprecedented accuracy.

The authors address signal integrity from architecture through high-volume production, thoroughly discussing design, implementation, and verification. Coverage includes

- New advances in passive-channel modeling, power-supply noise and jitter modeling, and system margin prediction
- Methodologies for balancing system voltage and timing budgets to improve system robustness in high-volume manufacturing
- Practical, stable formulae for converting key network parameters
- Improved solutions for difficult problems in the broadband modeling of interconnects
- Equalization techniques for optimizing channel performance
- Important new insights into the relationships between jitter and clocking topologies
- New on-chip measurement techniques for in-situ link performance testing
- Trends and future directions in signal integrity engineering

High-Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading hightech companies and universities: approaches that have never before been presented with this much practical detail. It will be invaluable to everyone concerned with signal integrity, including signal and power integrity engineers, high-speed I/O circuit designers, and system-level board design engineers.

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